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EXAMINER

DIAZ, JOSE R

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 09/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/256,265

Applicant(s)

KAO ET AL.

Examiner

José R Díaz

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 11 July 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1,2,8-10 and 16-22 is/are pending in the application.
- 4a) Of the above claim(s) 18-22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,8-10,16 and 17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Election/Restrictions***

➤ Newly submitted claims 18-22 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

This application contains claims directed to the following patentably distinct species of the claimed invention:

- Species I: a semiconductor device, wherein an erase gate is formed over sidewalls of one floating gate, as shown in Figure 1.
- Species II: a memory array wherein an erase gate is formed over portions of both first and second floating gate, as shown in Figure 2.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim is generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims

are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 18-22 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

### ***Claim Rejections - 35 USC § 112***

- The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

- Claims 1-2, 8-10 and 16-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 8, 9 and 16 are confusing due to the term "generally" used to describe how the floating gate, control gate, erase gate, source region, and drain region are formed in the device. It seems that Applicant, by using this term, is acknowledging that

the claimed device is well known in the art. Applicant is required to cancel the claim(s), or amend the claim(s) to clarify the confusion.

Claims 2, 10 and 17 are rejected due to their dependency on claims 1, 8 and 16, respectively.

***Claim Rejections - 35 USC § 102***

➤ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

➤ Claims 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Eitan et al. (US Patent No. 4,998,220).

Regarding claims 8-9, Eitan et al. teach a memory array comprising: a substrate (103) having a channel region (107a) (see Figs. 5 and 7a and Abstract); a first insulating layer (consider portion of the layer 105a, which is between the floating gate 104a and the channel region 107a); a floating gate (104a), a second insulating layer (consider portion of the layer 105a, which is on top of the floating gate 104a and between the control gate 106 and the erase gate 108); a control gate (106) having a portion disposed over a portion of said channel region (107a) and being separated therefrom by said second insulating layer, and wherein a portion of said control gate is disposed in facing relationship to a side surface of said floating gate and is separated from said floating gate by said second insulating layer (see Fig. 7a and Abstract), an erase gate (108) formed over one of the sides of said floating gate (104a) and being separated by said

second insulating layer (see Fig. 7a), a drain region (102a), a source region (110), (see Figs. 5 and 7a and Abstract); a plurality of rows and columns (see Fig. 5) of interconnected memory cells wherein the control gates are connected by a common word line (106) (see Fig. 5), the erase gates are connected by a common erase line (108) (see Fig. 5), the source regions are connected by a common source line (110) (see Fig. 5), and the drain regions are connected by a common drain line (see col. 6, lines 55-58); whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process (see col. 7, lines 14-17 and col. 7, lines 28-40).

***Claim Rejections - 35 USC § 103***

➤ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

➤ Claims 1-2, 10 and 16-17 rejected under 35 U.S.C. 103(a) as being unpatentable over Eitan et al. (US Patent No. 4,998,220) in view of Chang (US Patent No. 6,125,060).

Regarding claims 1 and 16, Eitan et al. teach a semiconductor device comprising: a substrate (103) having a channel region (107a) (see Figs. 5 and 7a and Abstract); a first insulating layer (consider portion of the layer 105a, which is between the floating gate 104a and the channel region 107a); a floating gate (104a), a second insulating layer (consider portion of the layer 105a, which is on top of the floating gate 104a and between the control gate 106 and the erase gate 108); a control gate (106) having a first portion disposed over a portion of said channel region (107a) and being separated therefrom by said second insulating layer, a second portion formed over a first one of said sidewalls and third portion formed over at least a portion of said top surface of said floating gate and being separated from said floating gate by said second insulating layer, said second portion having a surface substantially parallel to and opposing said first sidewall (see Fig. 7a and Abstract), an erase gate (108) formed over at least portion of said top surface of said floating gate (104a) and being separated by said second insulating layer (see Fig. 7a), a drain region (102a), a source region (110), (see Figs. 5 and 7a and Abstract); whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating

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gate to the erase gate through the Fowler-Nordheim tunneling process (see col. 7, lines 14-17 and col. 7, lines 28-40). However, Eitan et al. fail to teach an erase gate formed over a second one of said sidewalls of the floating gate. Chang teaches that is well known in the art to extend the erase gate (122) over a top and a sidewall of the floating gate (103) (see Fig. 1F). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Eitan et al. to include an erase gate formed over a top and a sidewall of the floating gate. The ordinary artisan would have been motivated to modify Eitan et al. in the manner described above for at least the purpose of manufacturing a semiconductor device having low currents for both program and erase operations.

Regarding claims 2, 10 and 17, Eitan et al. fail to teach an erase gate overlapping the floating gate. However, Chang teaches that is well known in the art to extend the erase gate (122) to cover portions of the control gate (101) and the floating gate (103) (see Fig. 1F). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Eitan et al. to include an erase gate that overlaps portions of the floating gate and the control gate. The ordinary artisan would have been motivated to modify Eitan et al. in the manner described above for at least the purpose of manufacturing a semiconductor device having low currents for both program and erase operations.

### ***Response to Arguments***

➤ Applicant's arguments with respect to claims 1-2, 8-10, and 16-17 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

➤ Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

### ***Correspondence***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00-5:00 Monday, Tuesday, Thursday and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for

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the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 746-3891 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD

September 17, 2002

A handwritten signature in black ink, appearing to read 'Eddie Lee', is positioned above the printed name and title.

EDDIE LEE  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800